REMARKS/ARGUMENTS

Reconsideration and allowance are respectfully requested. No new matter has been added by the amendments herein.

Rejections under 35 U.S.C. § 103

Claims 1-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. publication no. 2003/0033454 A1 to Walker et al. ("Walker") in view of U.S. publication no. 2002/0038393 A1 to Ganapathy et al. ("Ganapathy"). Applicants respectfully traverse this rejection.

Independent Claim 1

Independent claim 1 is amended only to incorporate all of the features of now-canceled dependent claim 2.

As amended, independent claim 1 recites associating with the output buffers and input buffers of DMA modules coupled in the chain at least one intermediate block to control data transfer between the coupled buffers. The Office Action compares the recited DMA modules with DMA controller 5 of Walker. It appears that the Office Action takes the position that, because DMA controller 5 has four ports A, B, C, D that can be interconnected, that DMA controller 5 can be configured as a number of different DMA modules. Nonetheless, and without opining on whether DMA controller 5 of Walker provides a plurality of DMA modules, Applicant submits that Walker still does not have the recited intermediate block to control data transfer between the coupled DMA module buffers.

The Office Action compares the recited intermediate block with a FIFO buffer as mentioned in paragraph 0038 of Walker. However, the FIFO buffer mentioned in paragraph 0038 does not control data transfer between the input and output buffers of two coupled DMA modules. Put another way, *the FIFO buffer of paragraph 0038 does not control data transferring between two of the ports A, B, C, D.* Instead, as described in paragraph 0038, the FIFO buffer is only used to buffer data between DMA controller 5 and a system bus: "Therefore a FIFO is implemented inside the DMA controller 5 to act as an elastic buffer so that if the

system bus is busy or the destination memory/module is busy, data currently in transit will not be lost."

For at least these reasons, it is submitted that Walker fails to teach or suggest the recited intermediate block to control data transfer between the coupled DMA module buffers.

And, the addition of Ganapathy to Walker fails to overcome this deficiency of Walker. Therefore, amended claim 1 is also allowable over both Walker and Ganapathy, either alone or in combination.

Independent Claim 5

Independent claim 5 as amended recites a processor coupled to a bus; and a plurality of respective DMA modules coupled together by the bus in a chain.

The Office Action alleges that Walker discloses a plurality of DMA modules coupled together in a chain. In taking this position, the Office Action is apparently comparing the recited DMA modules with the different combinations of ports A, B, C, D of Walker DMA controller 5. For instance, the Office Action refers to Walker paragraph 0030, which discloses that ports A, B, C, D may act as input or output ports, and that the various ports may be connected to each other in sixteen different ways.

Nonetheless, Walker does not teach or suggest that ports A, B, C, D are *coupled together by the bus*, as now recited in claim 1. Quite the opposite, Walker is concerned with keeping the bus free from DMA usage as much as possible. See, e.g., paragraphs 0005 and 0006 of Walker.

Nor does the addition of Ganapathy to Walker overcome this deficiency of Walker.

Moreover, the proposed modification to Walker by Ganapathy is not possible. The Office Action proposes to modify Walker by adding IP blocks to respective DMA modules as allegedly taught by Ganapathy. However, it is not possible to do this *while maintaining a chain arrangement* of the DMA modules in Walker (as required by claim 5).

Take an example in Walker an alleged first DMA module having ports A and B, and an alleged second DMA module is a module having ports C and D. For the device of Walker to work, at least two of the ports of must be coupled to the microprocessor (one for receiving instructions from the microprocessor and the other for sending results to the microprocessor). For the sake of example, it will be assumed that ports A and D are coupled to the

microprocessor. This leaves only two ports remaining, ports B and C. However, to arrange these alleged DMA modules into a chain as required by claim 5, then port B would need to be coupled to port C. Thus, there would be no further DMA ports remaining for coupling to IP blocks as proposed.

Even if somehow in this example only a single port needed to be coupled to the microprocessor (e.g., port A), then ports B and C would be coupled together (to provide the chain), thus leaving only port D remaining. However, the claim requires a plurality of IP blocks, one for each DMA module that is connected in a chain. Thus, a single port D is not sufficient for connecting at least two DMA modules to at least two IP blocks.

For at least these reasons, it is submitted that amended claim 5 is allowable over Walker and Ganapathy, either alone or in combination.

Independent Claim 11

New independent claim 11 is also allowable for at least similar reasons as discussed above with regard to claim 5.

Dependent Claims

The dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

For instance new claim 12 recites that the plurality of DMA modules comprises three modules. However, this is not possible in Walker since DMA controller 5 has only four ports. Since claim 12 requires at least three DMA modules, this means that the DMA modules must, as a group, contain at least six buffers (a first buffer and a second buffer, each).

Conclusion

All rejections having been addressed, Applicant respectfully submit that the present application is in condition for allowance, and respectfully solicit prompt notification of the same. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,
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